AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-5. canceled.

6. (currently amended): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, comprising:

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit,

a control circuit to which the second power source is supplied and which receives as inputs thereto a level conversion input signal and the level conversion output signal,

and a switching circuit which is disposed between a ground power source terminal of the level conversion core circuit and ~~the second~~ a ground power source and which is controlled by a third logic circuit, the third logic circuit generating a control signal under control of the first power source, wherein the control circuit is controlled by a control signal from the third logic circuit.

7. (previously presented): A level converting circuit in accordance with claim 6, wherein the third logic circuit controls the control circuit by a control signal from the third logic circuit, and the control circuit produces control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

8-14. canceled.

15. (currently amended): A level converting circuit in accordance with claim 7, wherein the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit, wherein an output signal of the NAND circuit is ~~produced to control a signal~~ one of said control circuit control signals.

16. (previously presented): A level converting circuit in accordance with claim 15, wherein the NAND circuit is of a CMOS circuit configuration and the p-MOS transistor to which the level conversion input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a high threshold value.

17. (previously presented): A level converting circuit in accordance with claim 15, wherein the NAND circuit is of a CMOS circuit configuration and the n-MOS transistor to which a control signal output of the third logic circuit is connected includes a source terminal connected to a GND power source.

18. (canceled).

19. (currently amended): A level converting circuit in accordance with claim 15, wherein the pull-up and/or pull-down circuit further comprises at least two p-MOSs each of which comprises a source terminal connected to the second power source, ~~and~~ a gate terminal connected to a control signal from the control circuit, and a drain terminal ~~of other pMOS being~~ connected to ~~each~~ one of the level conversion outputs; and at least two p-MOSs each of which comprises a source terminal connected to the second power source, ~~and~~ a gate terminal

connected to a control signal from the third logic circuit, and a drain terminal ~~of other p-MOS being~~ connected to ~~each~~ one of the level conversion outputs.

20. (previously presented): A level converting circuit in accordance with claim 15, wherein the pull-up and/or pull-down circuit further comprises at least two p-MOSs each of which comprises a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs; and a p-MOS comprising a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs.

21. (previously presented): A level converting circuit in accordance with claim 15, wherein the pull-up and/or pull-down circuit comprises at least two p-MOSs each of which comprises a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs, a p-MOS comprising a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs; and

an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level conversion outputs.

22. (currently amended): A level shifter in accordance with claim 15, wherein the pull-up and/or pull-down circuit comprises at least two p-MOSs each of which comprises a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of ~~the~~ two level shift

outputs; and an n-MOS comprising a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or an inverted signal of the control signal, and a drain terminal connected to one of the level shift outputs.

23. canceled.

24. (currently amended): A level shifter in accordance with claim 15, wherein the pull-up and/or pull-down circuit comprises at least two n-MOSs each of which comprises a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to ~~the~~ level shift outputs and at least two p-MOSs each of which comprises a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level shift outputs.

25-67. canceled.

68. (currently amended): A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, comprising:

a level conversion core circuit in which the second power source is supplied and which receives as an input a level conversion input signal and which outputs a level conversion output signal;

a control circuit to which the second power source is supplied and which receives a control signal from a third logic circuit and which outputs control signals; and

pull-up and/or pull-down circuit in which the second power source is supplied and which receives the control signals from the control circuit and a control signal from the third logic circuit and which ~~connects~~ is connected to a level conversion ~~an output to a level shift~~ output.